1.2 µW 41dB Ripple Attenuation Chopper Instrumentation Amplifier Using Auto-zero Offset Cancellation Loop

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***Abstract*—This paper presents a low power low noise capacitively-coupled chopper instrumentation amplifier (CCIA) for the recording of neural signals, including electroencephalogram (EEG) and electrocardiogram (ECG). Due to chopping technique, CCIA uses the proposed auto-zero offset cancelation loop to mitigate the output ripple. According to simulation results, the proposed CCIA obtains a ripple attenuation factor of 41.24 dB, the closed-loop gain is 40 dB with a bandwidth up to 800 Hz. A common-mode rejection ratio (CMRR) and a power rejection ratio are 108.9 and 87 dB, respectively, at the 50 Hz. The proposed CCIA, which was implemented in a 0.18 µm CMOS technology, occupies only 0.09 squared millimeters. The total current consumption of CCIA is 1.2 µA from a 1 V supply.**

Keywords—CCIA, chopper amplifier, output ripple, offset cancellation loop, insert *(key words)*

INTRODUCTION

Electroencephalogram (EEG) and electrocardiogram (ECG) recorded from the brain and the heart, is used for the healthcare, clinical purposes, and in the brain computer interfaces (BCIs) [1]. The neural signals have small amplitudes from 10 to 100 µV with a bandwidth from 0.5 to 150 Hz [2]. Therefore, in order to record these signals, the neural signals need to be applied the instrumentation amplifiers (IAs) before processing. However, when implemented by CMOS technology, the IAs is suffered from noise sources such as the flicker noise at low frequency. To achieve low noise, a chopping technique has been applied to IAs [3] - [5], as shown in Fig. 1. Therefore, 1/*f* of the IAs is chopped to the high frequency, outside of the bandwidth of the IAs.

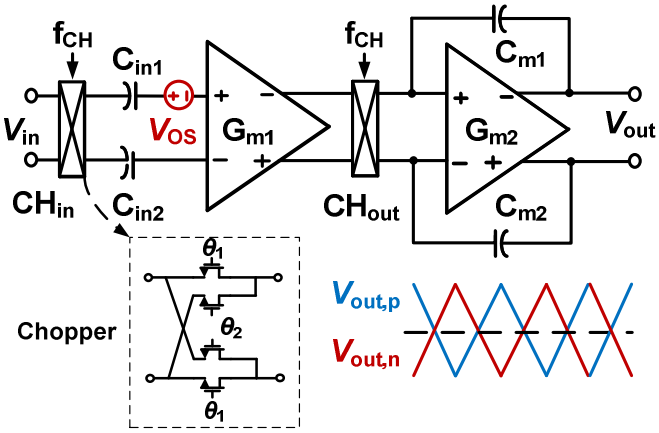

Fig. 1. Schematic of the chopper amplifier.

Unfortunately the intrinsic offset V_{OS} caused by process variation at the input stage is up-modulated to chopping frequency by the chopper output (CH_{out}), then integrated by the output stage become the output ripple. Several approaches [6]-[8] are added into the capacitively – coupled chopper instrumentation amplifier (CCIA) to address this issue.

In this paper, a CCIA using a proposed auto-zero offset cancelation loop (A-OCL) is presented. The proposed CCIA achieves a ripple attenuation factor of 41 dB and a closed-loop

gain of 40 dB, drawing 1.2 µA from a 1 V supply. In addition, the proposed CCIA utilizes the T-capacitance network for the negative feedback loop to achieve a high efficient silicon chip area. By implementation in a 180 nm CMOS technology, the CCIA occupies a chip area of 0.22 x 0.41 mm^2.

AMPLIFIER ARCHITECURE

Fig. 2 shows the overall structure of the proposed CCIA. A folded cascode (FC) amplifier is used in the first stage labelled G_{m1}, while the second stage, labelled G_{m3}, employs a common source (CS) amplifier to create a high output swing. In order to achieve phase margin of 60 degrees, the Miller capacitors $C_{m1,2}$ of 1.5 pF are utilized. At the V_{DD} of 1 V supply, the biased current for G_{m1}, G_{m2} is 980 nA, including a common mode feedback CMFB, and 180 nA, respectively, to achieve a DC gain of about 100 dB. The closed-loop gain of 40 dB is defined by the ratio of input capacitance C_{in} and the feedback capacitance C_{fb}. In this wok, a T-capacitor network [9] is used to represent C_{fb} that leads to a reduction of C_{in} from 21 [10] pF to 2 pF. Therefore, the proposed CCIA occupies chip area efficiency. The resistors $R_{b1,2}$, which is implemented by NMOS pseudo resistor as shown in Fig. 2, is employed to bias for G_{m1}. The electrode offset generated at the input is prevented by a high pass filter, which is formed by $R_{off1,2}$ and $C_{off1,2}$.

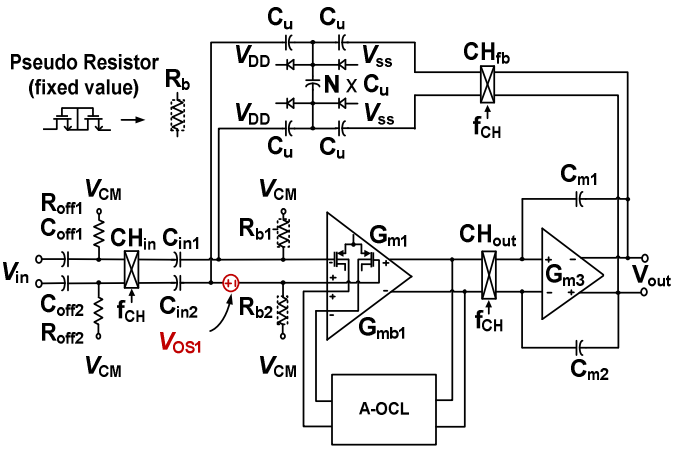

Fig. 2. Schematic of the proposed CCIA using A-OCL.

As shown in Fig.2, G_{m1} is associated with an intrinsic offset V_{OS1} caused by the process variation. V_{OS1} is up-modulated by the chopper output CH_{out} and integrated by Miller stage to generate the output ripple. In order to mitigate the output ripple, the proposed auto-zero ripple reduce loop (A-OCL) is added into the CCIA.

Fig. 3 shows the schematic of A-OCL which includes a RC low-pass filter and a two-stage opamp as labelled G_{m2}. The A-OCL senses the offset at the G_{m1}'s output, then amplifies by G_{m2} to create output voltage V_{OCL}. The V_{OCL} is applied to the buck of the differential pair input MOS transistors of G_{m1} to compensate V_{OS1}. However, G_{m2} also has an intrinsic offset V_{OS2} due to process mismatch during fabrication. The V_{OS2} also generates the output ripple, hence it must be reduced by proposed auto-zero approach. The operation of switches $S_{1,2}$ are controlled by $f_{s1,2}$, as shown in Fig. 3, which is chosen of 50% chopping frequency. The timing diagram is shown in Fig. 3, $f_{s1,2}$ consists of a charging phase φ_1 and an auto-zero phase φ_2 (balanced offset phase).

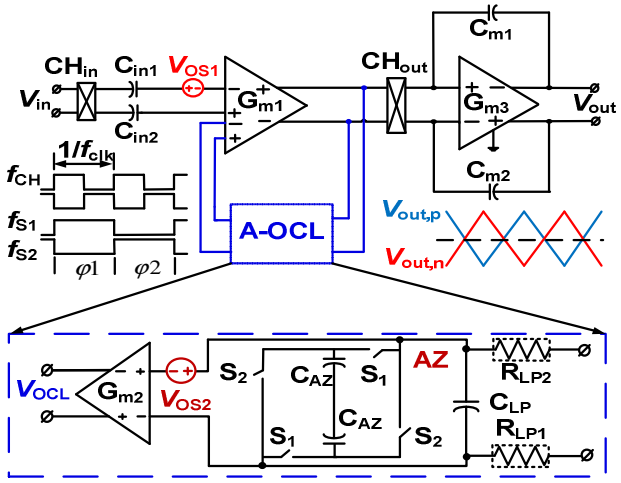

Fig. 3. Schematic of the proposed A-OCL.

The auto-zero loop independence on f_{chop}, it is not effect to operated rippled reduction. During φ1, the V_{OS2} is charged to stored capacitor C_{AZ}. During φ_2, the charged voltage in C_{AZ} is charged to opposite input of G_{m2}, thus DC voltage at the differential input of G_{m5} is balanced. This means that offset voltage of G_{m5} is suppressed by its.

CIRCUIT IMPLEMENTATION

A. *Buck-control forded-cascode amplifier in the first stage*

As we well know that the buck terminal behaves as a second gate. Therefore, in this design, the buck of the input differential pair CMOS is employed to control the channel [11]-[13]. Fig. 4 shows the schematic of the first stage G_{m1} using buck control input differential pair CMOS transistors. Therefore, the output voltage of OCL, V_{OCL}, is applied to buck of CMOS transistors $M_{1,2}$ to compensate V_{OS1}. The input CMOS transistors $M_{1,2}$ is worked in subthreshold region for low power and achieve high transconductance.

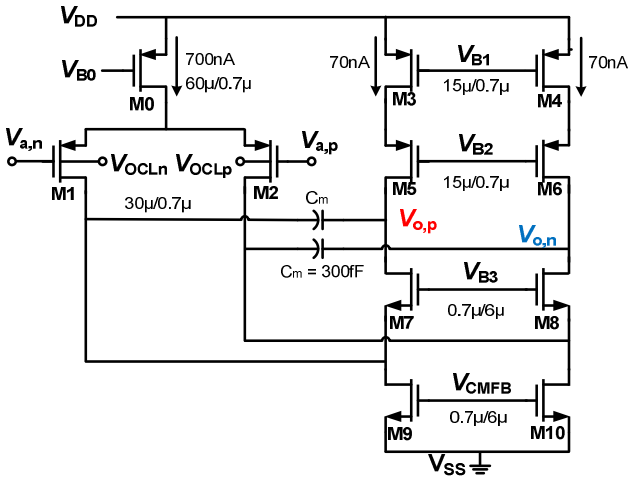

Fig. 4. Schematic of folded-cascode opamp G_{m1} using buck control input differential pair CMOS transistors.

Fig. 5 shows the statiscal distribution open loop gain of G_{m1} obatained after running 200 Monte Carlo simulations with considersing random mismatch and process variations. The result shows that the mean value of G_{m1}'s gain is 67.5 dB with a standard deviation of 0. 5 dB.

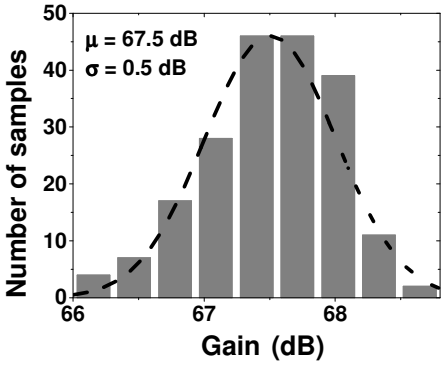

Fig. 5. Statistical distribution of the gain of G_{m1}.

The schematic of two-stage amplifier, G_{m2}, in A-OCL is shown in Fig. 6. G_{m2} uses a two-stage opamp to achieve a high gain. Moreover, the output stage utilizes a class-A amplifier to achieves the high output swing. Run 200 Monte Carlo simulation considering process variation and random mismatch, Fig. 7 shows the Monte Carlo simulated gain result of G_{m2}, the mean of the DC gain of two-stage amplifier achieves around 78.6 dB with a standard deviation of 0.84 dB by drawing current of 30 nA from 1 V supply.

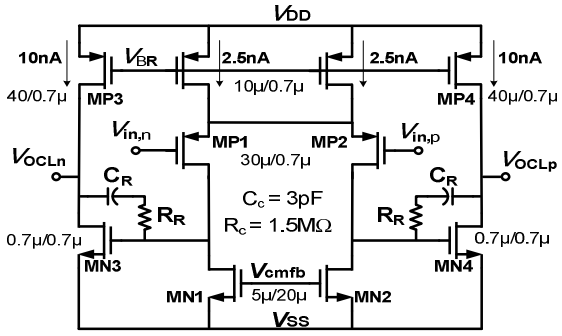

Fig. 6. Schematic of a two-stage opamp G_{m2} in A-OCL.

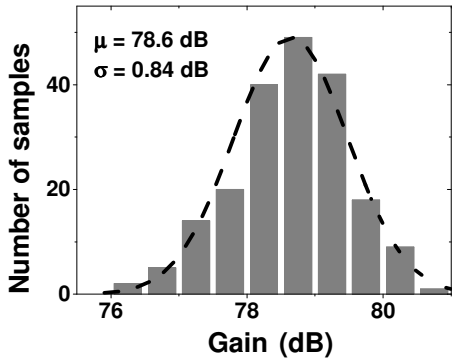

Fig. 7. Monte Carlo simulated gain result of G_{m2}.

Simulation Results

Fig. 8 shows the layout of the proposed CCIA using A-OCL which is realized in a 180 nm CMOS technology. The layout chip occupies 0.22 x 0.41 mm^2 silicon area. Fig. 9 shows the simulated frequency response of the CCIA with bandwidth of up to 800 Hz. During simulated, the RC-off chip high pass filter is not included, the closed-loop gain of CCIA of 40 dB is achieved without a high pass corner at low frequency.

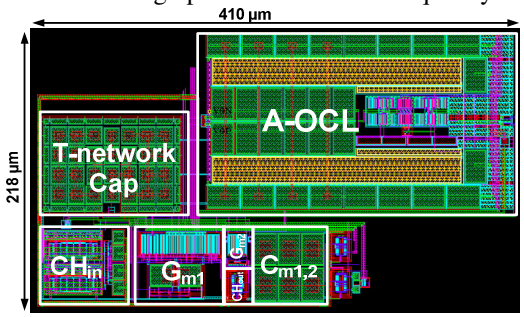

Fig. 8. Schematic of a two-stage opamp G_{m2} in A-OCL.

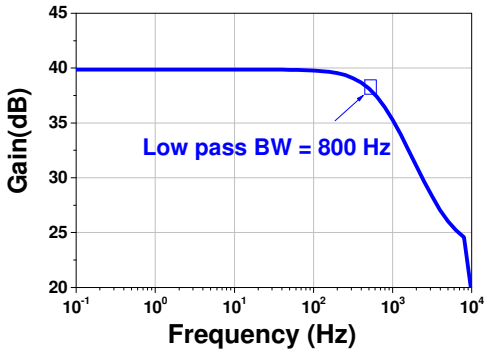

Fig. 9. Simulated frequency response of the proposed CCIA.

Run 200 samples Monte Carlo simulations considering the process variation and devices mismatch. Fig. 10 shows simulated results of the power suppy rejection ratio (PSRR) of the CCIA. The mean value of PSRR is 87 dB with the standard deviation of 24.7 dB at the frequency of 50 Hz. Fig. 11 shows simulation results of the common mode rejection ratio (CMRR). The average value of CMRR is 108 dB with the standard deviation of 39.5 dB checked at the frequency of 50 Hz.

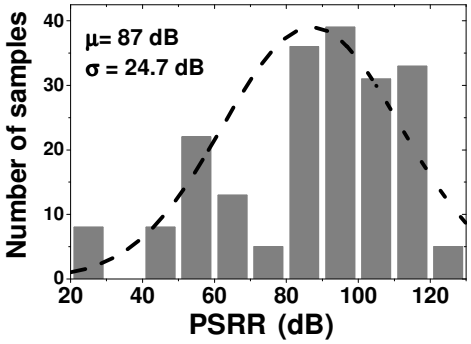

Fig. 10. Monte Carlo simulated PSRR result of CCIA.

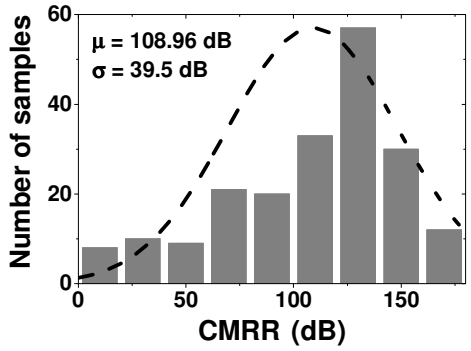

Fig. 11. Monte Carlo simulated CMRR result of CCIA.

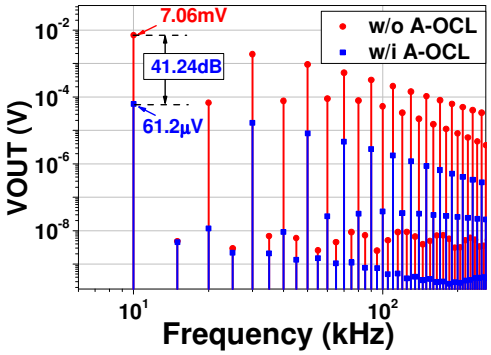

Fig. 12. Spectrum output voltage in cases with and without A-OCL.

Fig. 12 shows the simulation results of the output signal spectrum of the CCIA with and without A-OCL. The V_{OS1} is set at 5 mV, the output ripple is 7.06 mV when A-OCL is disabled. White the A-OCL is enabled, the oupt ripple is reduced to 61.2 μV, corresponding to the ripple attenuation factor of 41.24 dB.

V. Conclusion

This paper presents a proposed CCIA using A-OCL to achieve the ripple attenuation factor of 41 dB. The T-capacitance network is used to apply to the capacitance negative feedback in the CCIA, therefore, the input capacitance of 2 pF can be used, that leads to a reduction of the silicon chip area. The proposed CCIA offers a closed-loop gain of 40 dB, PSRR of 87 dB, and CMRR of 109 dB by drawing current of 1.2 μA from a 1 V supply.

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