A study of 10-bit 2-MS/s Successive Approximation Register ADC with low power in 180nm technology

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***Abstract*— This paper presents Successive Approximation Register (SAR) ADC design in 180nm TSMC technology with high speed and low power. At a 1.8-V supply and 2 MS/s, our design achieves an SNDR of 59.5 dB, ENOB 9.59 bit and consumes 1.17 mW, resulting in a figure of merit (FOM) of 64 fJ/conversion-step. To attain the mentioned results, the SAR architecture is proposed to use SAR ADC fully differential with S/H circuit, Capacitive DAC, Dynamic latch comparator, SAR Logic.**

***Keywords*— ADC, SAR ADC, DAC.**

I. INTRODUCTION

The Analog to Digital Converter (ADC) has been introduced and developed for a long time ago. It plays an important role in many devices which helps us to approximate the real-world data in a digital standpoint. In the early days, due to the restriction on the semiconductor devices, the ADC design was difficult to meet high resolution, high speed and low power targets. However, thanks to the advancement of technology, the CMOS is scaling and becoming faster and more integrated.

Many ADCs such as Flash ADC, SAR ADC, Pipeline ADC and Delta-Sigma ADC, … have been implemented depend on the application [1]. For instance, the advantage of Flash ADC is high speed but it costs a large area leading to limited resolution. Compared to other ADC structures, thanks to the advantages of Successive Approximation Register (SAR) ADCs including low power consumption, medium resolution, high accuracy, high speed and smaller die area to integrate in CMOS technology [2], SAR ADC has attracted more research and becomes one of the most popular ADCs today.

Generally, the working of SAR architecture is based on the binary search algorithm to approximate the output following the input [3]. However, the switching power on capacitive DAC and the comparator are considered as major causes leading to the energy consumption. In order to reduce the power consumption and the area, the Split DAC array architecture and the dynamic latch comparator are proposed to be used in this paper. The split capacitor method reduces switching energy by 37%, the energy-saving method reduces energy consumption by 56% [4] and the area reduces by 93% compared to the traditional DAC. Besides, using clock frequency in the dynamic latch comparator reduces the energy consumption by 30% (result is measured in this paper).

The proposed SAR ADC consists of a binary weighted capacitor array, a dynamic latch comparator and a SAR logic as shown in Fig.1 [5] and implement with fully differential structure.

Last but not least, the benefits of fully differential structure could be listed as follows. The first, it cancels noise at common-mode inputs. The second, it provides higher gain (6,02dB) comparing to single-ended structure. Therefore, using fully differential structure brings many advantages to achieve higher ENOB, higher speed for SAR ADC design.

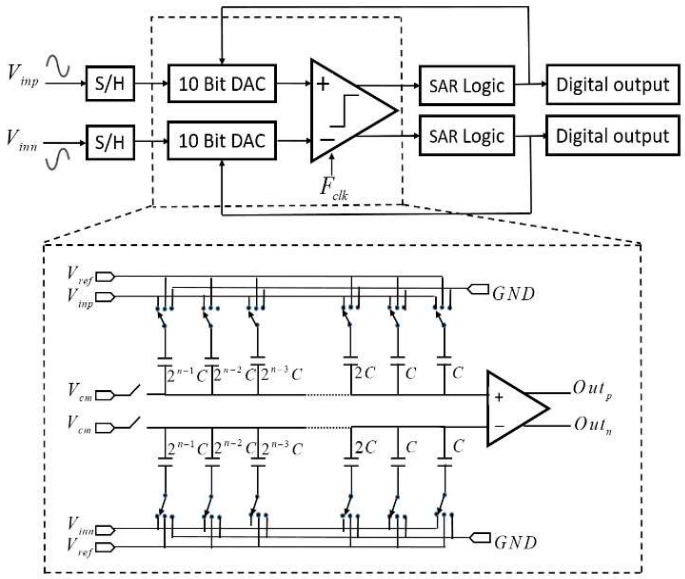

Fig.1 Conventional SAR ADC architecture with charge redistribution DAC configuration

The remainder of this paper is organized as follows. Section II gives the details of ADC architecture and our design. After presenting experimental results and brief discussion of design in section III, we conclude our paper in section IV.

II. ARCHITECTURE AND CIRCUIT DESIGN

The SAR ADC fully differential reduces supply noise and has good common-mode noise rejection. The fundamental building blocks are the comparator, sample-and-hold (S/H), capacitor network, and successive approximation registers.

A conversion of SAR ADC includes four modes: Reset mode, Sample mode, Hold mode and re-distribution mode [6]. In the resetting mode, all the capacitors in the DAC will be reset so that the conversion will get more linear by avoiding many non-linearity in terms of wrong values in the capacitors. In the sampling mode, all the top plates of the capacitors get connected to Vcm level, all the bot plates of the capacitors get connected to Vin. In the holding mode, all the top plates of the capacitors get disconnected to Vcm level and all the bot plates

get connected to Gnd. In the next re-distribution mode, all the switch from MSB capacitor to LSB capacitor will be turn on respectively and receive feedback from the comparator to approximate the Vin voltage. In the final conversion, the results (10-bit) will be latch in the next Vin voltage.

A. Sample and hold circuit

To achieve high speed, S/H circuit is proposed to be used as follows Fig.2.

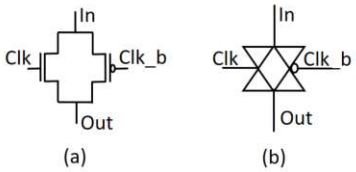

Fig. 2. (a) Transmission gate switch and (b) Symbol of transmission gate switch

B. Capacitive DAC

The DAC is a heart of the SAR ADC. It is differential and integral non-linearity will directly be reflected in the transfer function of the ADC. Fig.3 illustrates the convention of traditional 3-bit CDAC.

Initially, the sampling switch will be connected to array capacitors, the negative array will be connected to Vinn and the positive array will be connected to Vinp. At this time, the capacitors are charged with the corresponding power level:

$$\begin{cases} Q_{samp} = Q_{+} = \left(V_{CM} - V_{inp}\right).8C \\ Q_{samn} = Q_{-} = \left(V_{CM} - V_{inn}\right).8C \end{cases} \quad (1)$$

In the second period, the MSB switch will be turned on, the negative MSB will be connected to GND and the positive MSB will be connected to VDD. Therefore, we have:

$$\begin{cases} Q_{samp} = Q_{1p} = \left(V_{+} - V_{REF}\right).4C + \left(V_{+} - 0\right).\left(2C + C + C\right) \\ Q_{samn} = Q_{1n} = \left(V_{-} - 0\right).4C + \left(V_{-} - V_{REF}\right).\left(2C + C + C\right) \end{cases} \quad (2)$$

"(1)" associate with "(2)", we have:

$$\begin{cases} V_{+} = V_{CM} - V_{inp} + \left(\frac{1}{2}.1\right)V_{REF} \\ V_{-} = V_{CM} - V_{inn} + \left(\frac{1}{2}.1\right)V_{REF} \end{cases}$$

If $V_{+} > V_{-}$, we retain the connect of negative and positive MSB. It is mean we receive a bit 1. If $V_{+} < V_{-}$, we reverse the connect of MSB and receive a bit 0.

Assume that $V_{+} > V_{-}$, we receive a bit 1. At the third period, switch MSB-1 will be turned on and continue connecting the negative MSB-1 to GND and the positive MSB-1 to VDD. We have:

$$\begin{cases} Q_{samp} = Q_{2p} = \left(V_{+} - V_{REF}\right).\left(4C + 2C\right) + \left(V_{+} - 0\right).\left(C + C\right) \\ Q_{samn} = Q_{2n} = \left(V_{-} - 0\right).\left(4C + 2C\right) + \left(V_{-} - V_{REF}\right).\left(C + C\right) \end{cases} \quad (3)$$

With "(1)" and "(3)", we have:

$$\begin{cases} V_{+} = V_{CM} - V_{inp} + \frac{3}{4}.V_{REF} = V_{CM} - V_{inp} + \left(\frac{1}{2}.1 + \frac{1}{4}.1\right)V_{REF} \\ V_{-} = V_{CM} - V_{inn} + \frac{1}{4}.V_{REF} = V_{CM} - V_{inn} + \left(\frac{1}{2}.0 + \frac{1}{4}.1\right)V_{REF} \end{cases}$$

The comparator still does such second period. Hence, using the induction method, the output voltage of the DAC fully differential gives by:

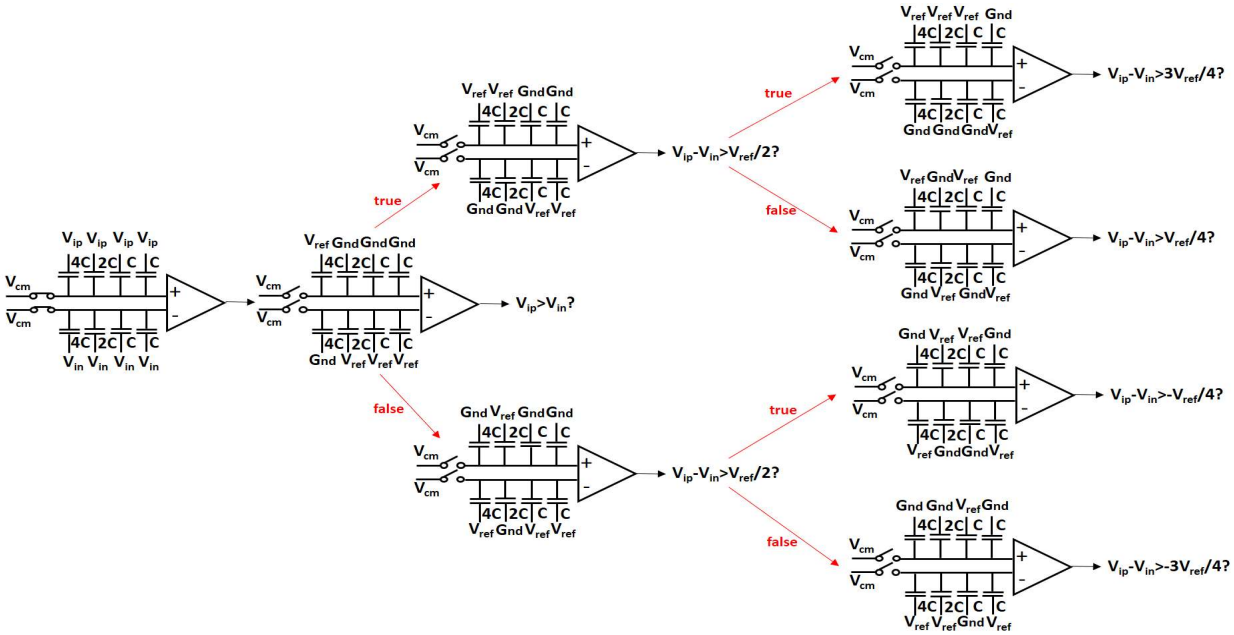

Fig.3 Conventional switching procedure of charge redistribution DAC

$$\begin{cases} V_{DAC+} = V_{CM} - V_{inp} + \sum_{k=0}^{N-1} B_k \cdot \frac{V_{ref}}{2^{N-k}} \\ V_{DAC-} = V_{CM} - V_{inn} + \sum_{k=0}^{N-1} \overline{B}_k \cdot \frac{V_{ref}}{2^{N-k}} \end{cases}$$

With n is the number of bits resolved by charge redistribution DAC, Vcm is half of Vref.

To reduces the area of DAC from 512C (with charge redistribution DAC) to 16C in Fig. 4, Split DAC architecture is proposed to be used [7]. With this architecture, the design of SAR ADC can achieve 16 bit resolution.

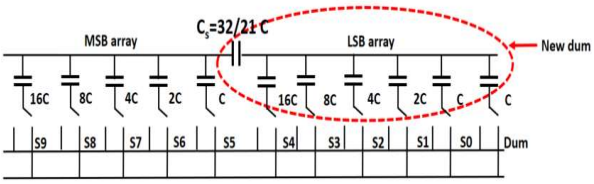

Fig.4 The split DAC

We divide Charge redistribution DAC into two arrays. One calls 5-bit MSB, the other is 5-bit LSB and compensate between them a capacitor Cs. We have therefore two small 5-bit charge redistribution DAC.

The new total dummy capacitor has a value of the least capacitor MSB array. So, Cs is capacitor reducing scale of DAC, can be given by:

$$\frac{1}{C_{new\_dum}} = \frac{1}{C} = \frac{1}{C_s} + \frac{1}{\sum C_{LSB}}$$

$$\Rightarrow C_s = \frac{1}{\frac{1}{C} - \frac{1}{(16+8+4+2+1+1)C}} = \frac{32}{31}C$$

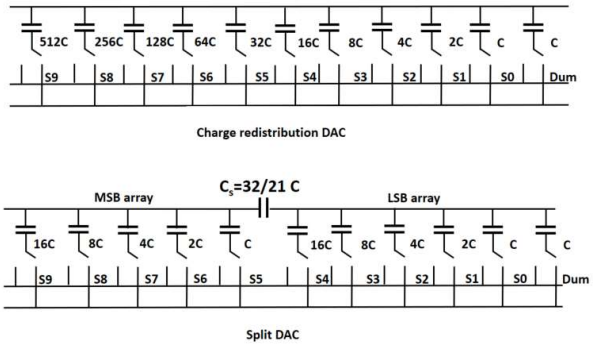

Fig. 5. Compare between the charge redistribute-ion DAC with The Split DAC

C. Comparator

The comparator needs to be designed to achieve high gain, high bandwidth, low offset and low power. The purpose of the architecture is dynamic latch comparator. The dynamic latch comparator has three stage including: preamplifier, regenerative latch, and SR latch.

The preamplifier has a large enough input signal amplification function. It should have wide bandwidth and small gain to achieve high speed. The preamplifier decreases the effect of offset voltage error due to device mismatch and also reduces the disturbance due to kick back noise. The proposed of the preamplifier is shown in Fig.6.

The regenerative latch has a function to determine the logic level, the ability to distinguish mV signals. Fig.7 shows the proposed of the regenerative latch. The proposed architecture consists of transistors M1, M2, M3, M4 as the input circuitry; transistors M0, M5, M6, M7, M8, M9, M10, M11 and M12 are configure of latch circuitry. Transistors M3, M4 generate the positive feedback to allow the faster switch at the output. Transistors M11, M12 reduce the offset voltage.

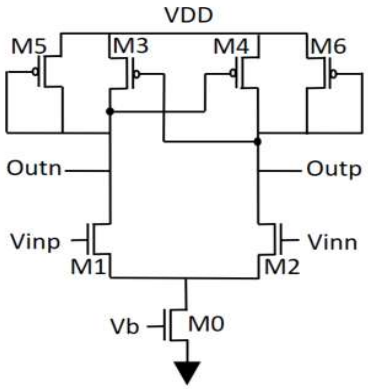

Fig. 6. The proposed preamplifier

The operation of the proposed comparator is divided two phases. When Vlatch = VSS, no current in transistor M0; transistors M9, M10, M11, M12 turn on to connect the output voltage Outn and Outp to VDD. When Vlatch = VDD, transistor M0 appears current, transistors M9, M10, M11, M12 turn off to allow the comparison of the differential input voltage. In this case, assuming that Vinp > Vinn, Node Outn discharges faster than Outp. Consequently, Outn falls down VDD-|Vthn| before Outp to make transistor M8 turn on by inverters of latch generation. Thus, Outp pulls to VDD and Outn discharges to VDD. If Vinp < Vinn, the circuit works vice versa.

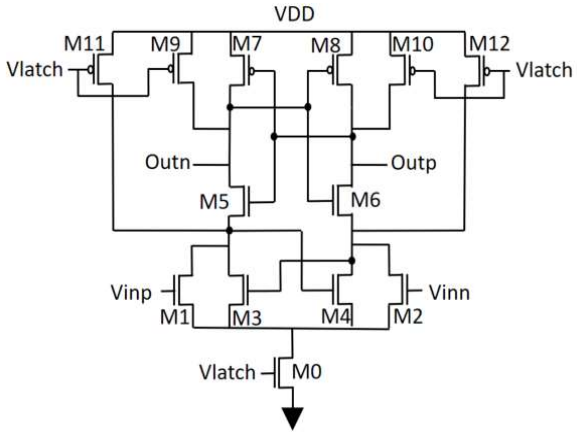

Fig. 7. The proposed of regenerative latch

D. SR Latch

When the regenerative latch turns on, the logic level is determined. We will latch this value when the regenerative turns off. In this case, NAND latch is used due to Outn = Outp

=VDD (coincide with the truth table of NAND latch showed in Fig. 8).

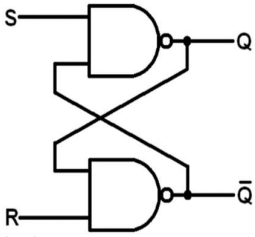

Fig. 8 NAND latch

E. SAR Logic

The SAR logic shown in Fig. 9, was designed to give a digital code to the DAC based on the output from the comparator.

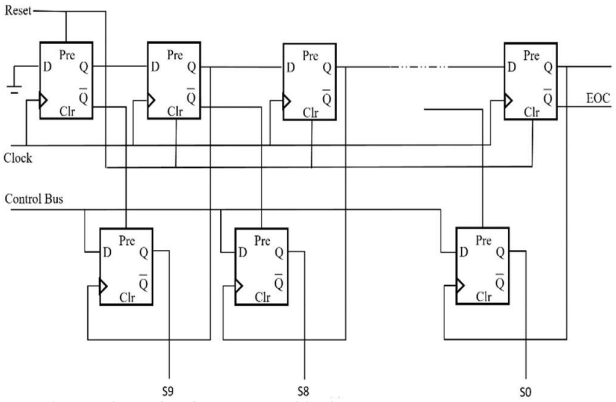

Fig. 9 Schematic of SAR control logic

It consists of two stages. The first stage generates continuous translation pulses. The second stage uses pulses prior to latch values of the comparator and give the ADC output at the end of the operation together with the End of Conversion (EOC) signal.

The symbol A0 to A9 are the values that have been compared and returned for control. The symbol S0 to S9 are digital output in sequence. The convention of SAR logic is shown in Fig.10.

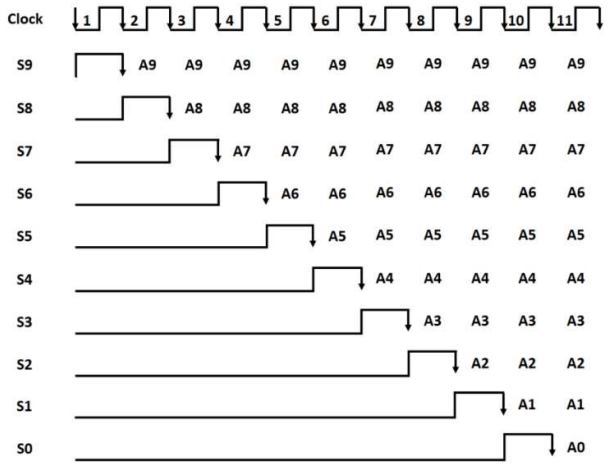

Fig. 10 Timing diagram of SAR control logic

III. EXPERIMENTAL RESULTS

The simulation results are implemented at Ho Chi Minh City University of Technology (HCMUT) lab - Viet Nam and measured in Cadence tool with 180nm TSMC technology.

The evaluation results include:

- Static performance: Differential nonlinearity (DNL), Integral nonlinearity (INL).
- Dynamic performance: Signal to Noise Distortio--n (SNDR), Spurious-free dynamic range (SFDR), Effective number of bits (ENOB)
- And other performance results.

A. Static Performance

The measured differential nonlinearity (DNL) and integral nonlinearity (INL) of the proposed ADC are shown in Fig. 11. The peak DNL and INL are -0.5 to 0.2 LSB and -0.3 to 0.3 LSB, respectively.

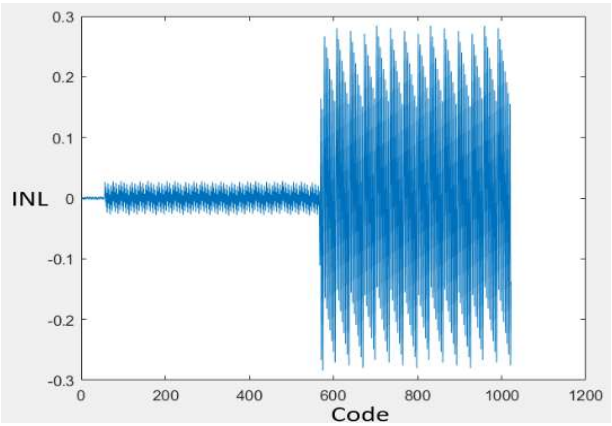

Fig. 11-a INL measurement

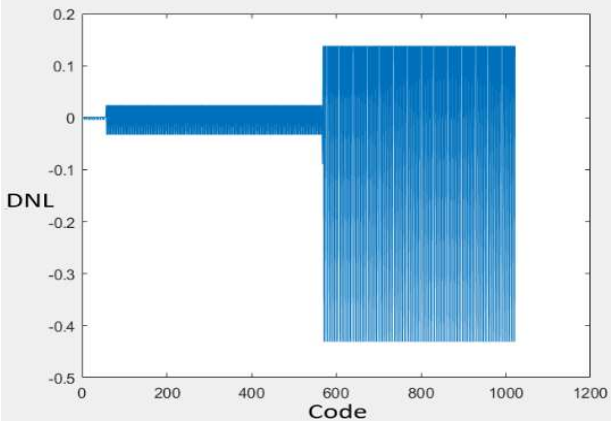

Fig. 11-b DNL measurement

B. *Dynamic Performance*

Fig.12 shows the measured FFT spectrum with an input frequency of close to 50 Khz at a 1.8-V supply and a 2-MS/s sampling rate. The measured SNDR and SFDR are 59.5dB and 77.9 dB, respectively. The resultant ENOB is 9.59 bits.

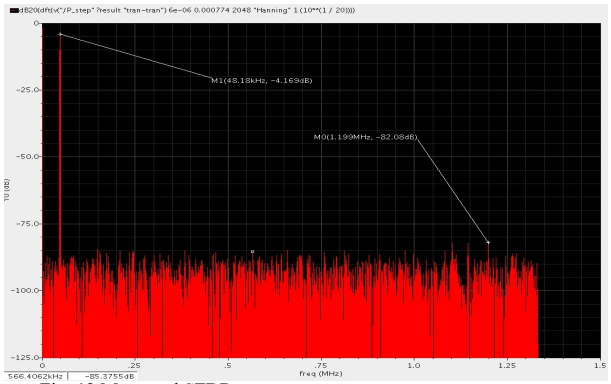

Fig. 12 Measured SFDR

At a 1.8-V supply, the power consumption was measured of 1.17mW. Table I shows results of this work and compare with other works.

Parameters	Hieu[5]	Shreeniwas[8]	Colleta[9]	Hu[10]	This works
Technology	180nm CMOS	70nm CMOS	180nm CMOS	65nm CMOS	**180nm CMOS**
VDD	1.8V	1.2V	1.1V	1V	**1.8V**
Resolution	10 bits	8 bits	8 bits	10 bits	**10 bits**
Samples	25 MS/s	250 MS/s	10 kS/s	1 kS/s	**2MS/s**
Power	3.83mW	1.3mW	12.4mW	0.13mW	**1.17mW**
DNL	-0.7/0.7	-	-0.70 / 0.20	-0.17/0.28	**-0.5/0.2**
INL	-3.6/3.6	-	-1.00/0.2	-0.27/0.81	**-0.3/0.3**
FOM	374.4 fJ/conv	20 fJ/conv	227 fJ/conv	63fJ/conv	**64 fJ/conv**
Architecture	SAR	SAR	SAR	SAR	**SAR**

Table I Comparison to STATE-OF-THE-ART works

IV. Conclusion

The 10-bit 2MS/s SAR ADC using separated clock frequency has been introduced in this work. At a 1.8-V supply and 2 MS/s, our design achieves an SNDR of 59.5 dB, ENOB 9.59 bit and consumes 1.17 mW, resulting in a figure of merit (FOM) of 64 fJ/conversion-step. Therefore, this proposed SAR ADC architecture is suitable for low power and high speed application such as power management and video processing. In the future, the calibration techniques will be utilized in this work in order to improve the DNL and INL.

Acknowledgements

We acknowledge the support of time and facilities from Ho Chi Minh City University of Technology (HCMUT), VNU-HCM for this study.

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